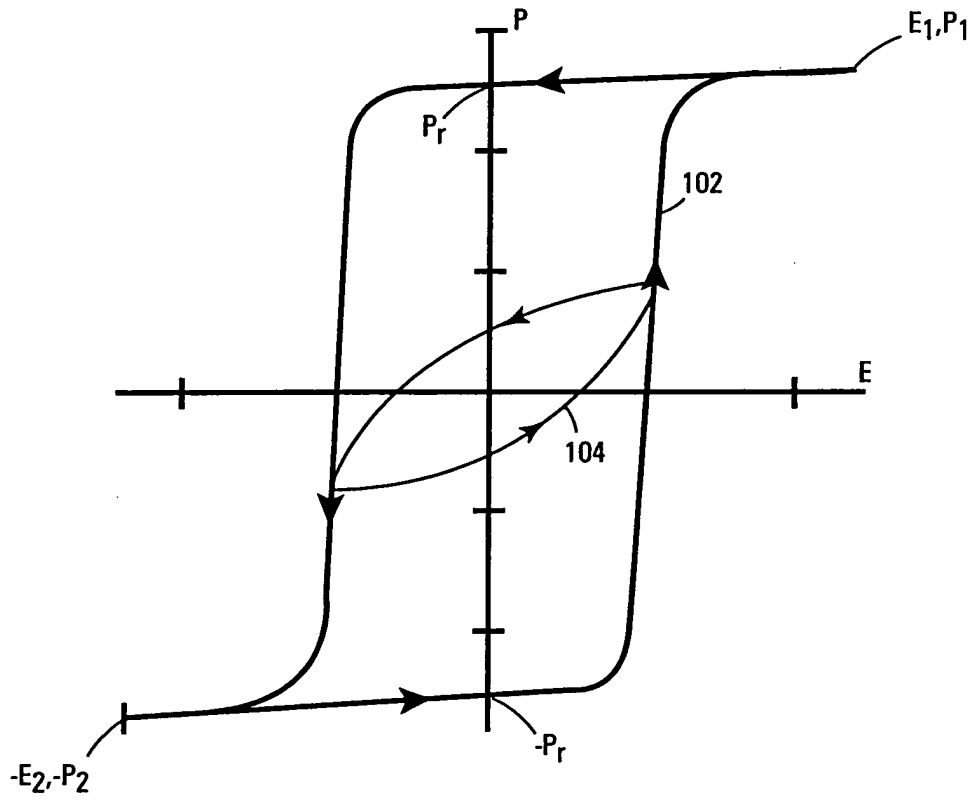


Fig. 1
Prior Art

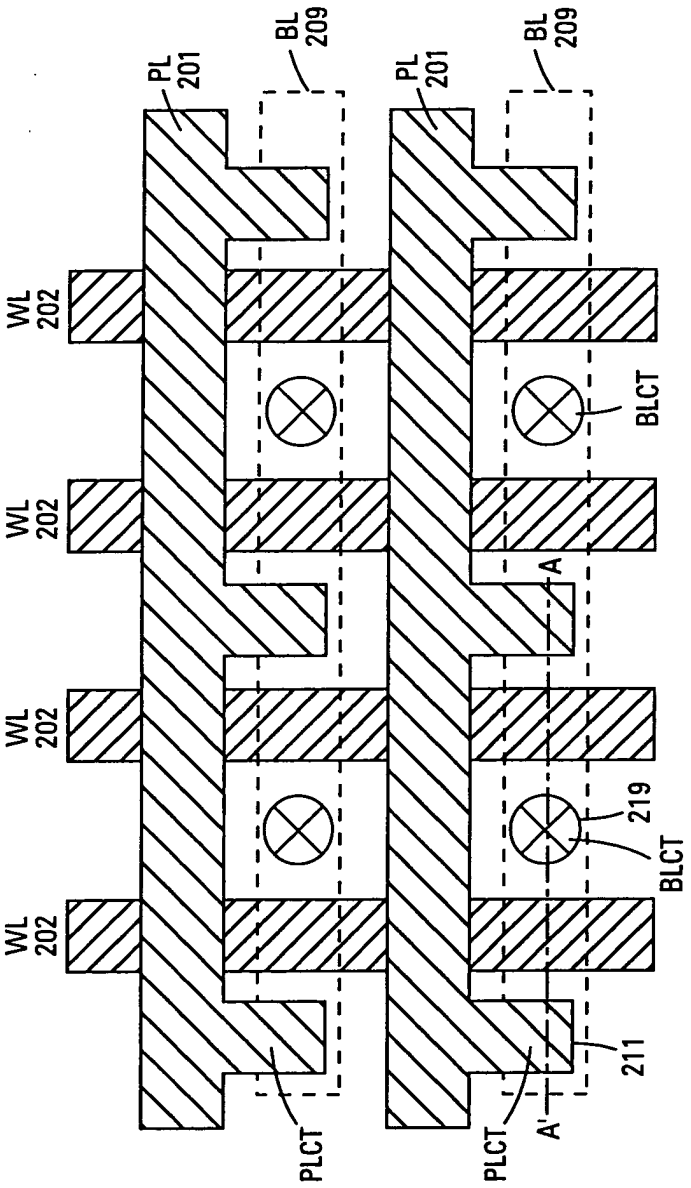
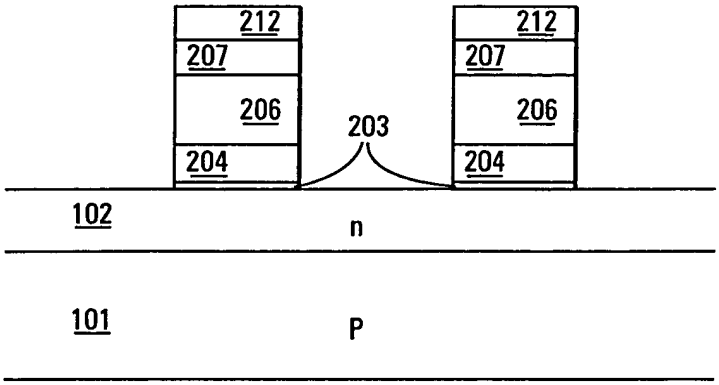

PL
201
BL
209
PL
201
BL
209
WL
202
WL
202
WL
202
WL
202
BLCT
A
219
BLCT
211
PLCT
PLCT
A'

Fig. 2


212
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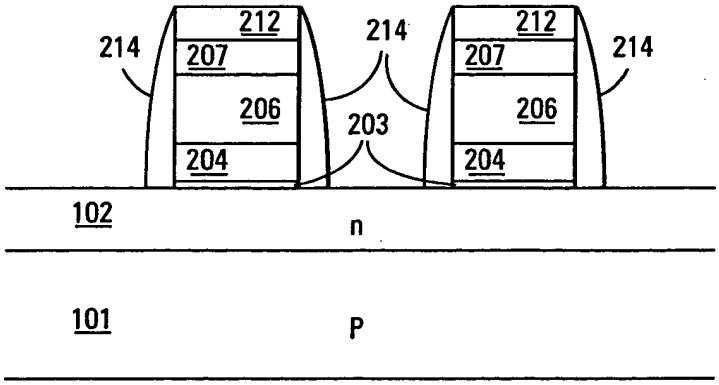
206
204
203
212
207
206
204
102
n
101
P

Fig. 3A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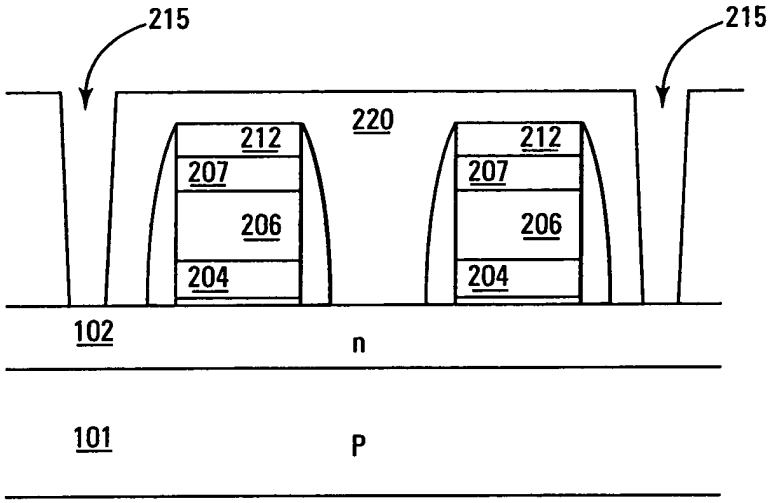
204
214
102
n
101
P

Fig. 3B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215
220
212
207
206
204
212
207
206
204
102
n
101
P

Fig. 3C

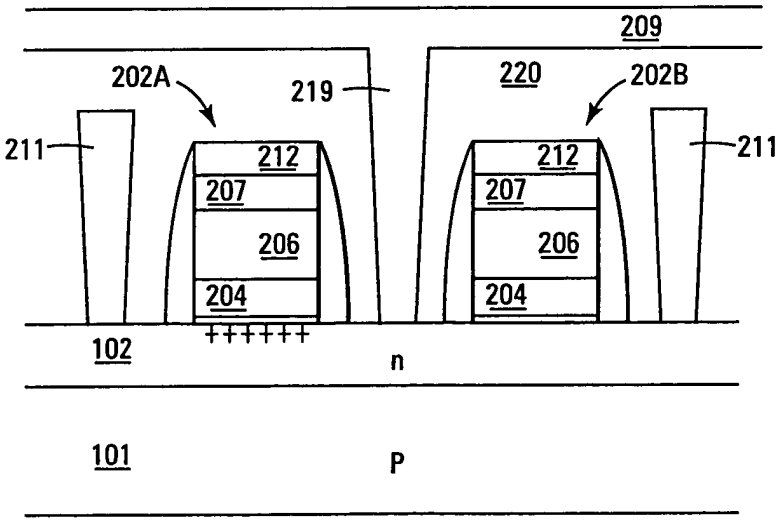
209
202A
219
220
202B
211
211
212
207
206
204
212
207
206
204
++++++
102
n
101
P

Fig. 3D

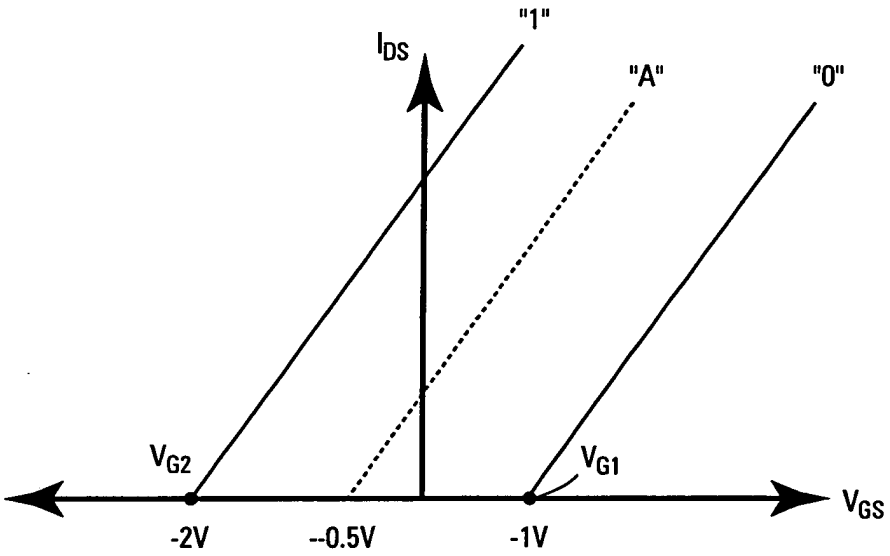

Fig. 4

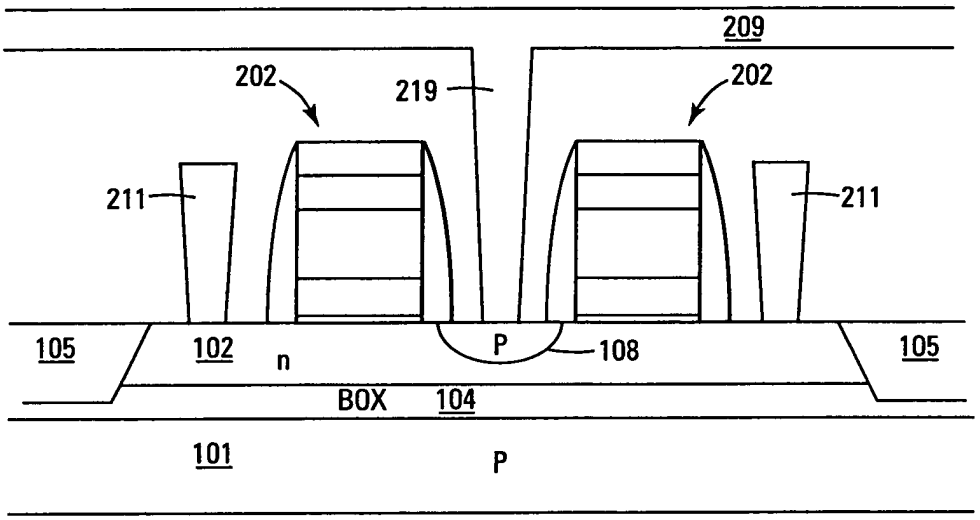

Fig. 5

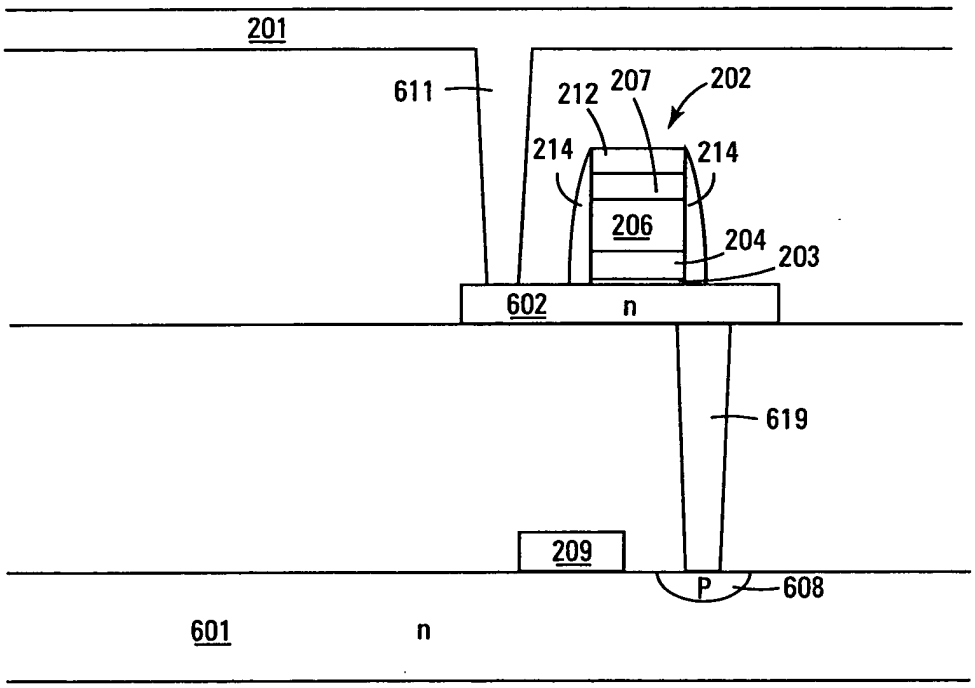

Fig. 6

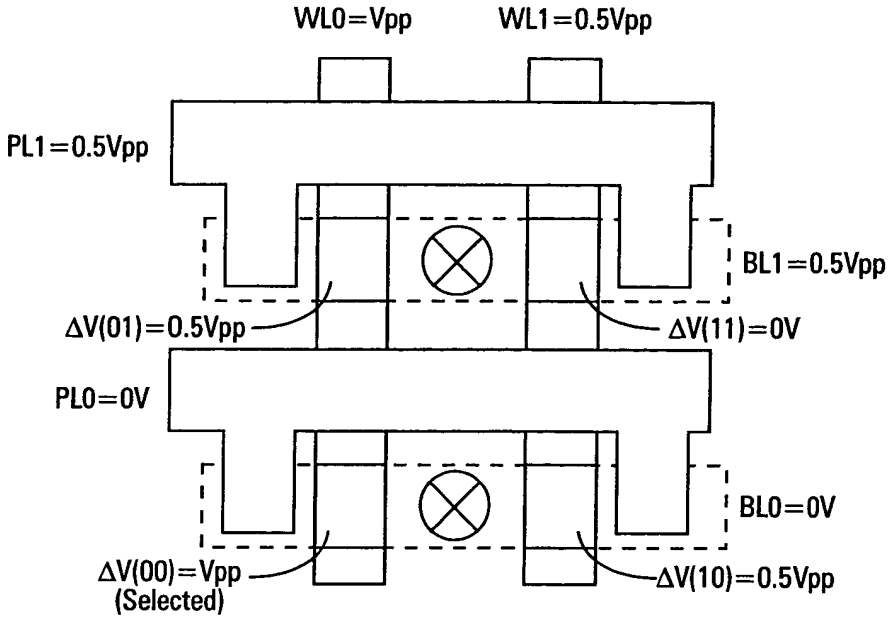
WL0=Vpp
WL1=0.5Vpp
PL1=0.5Vpp
BL1=0.5Vpp
ΔV(01)=0.5Vpp
ΔV(11)=0V
PL0=0V
BL0=0V
ΔV(00)=Vpp
(Selected)
ΔV(10)=0.5Vpp

Fig. 7A

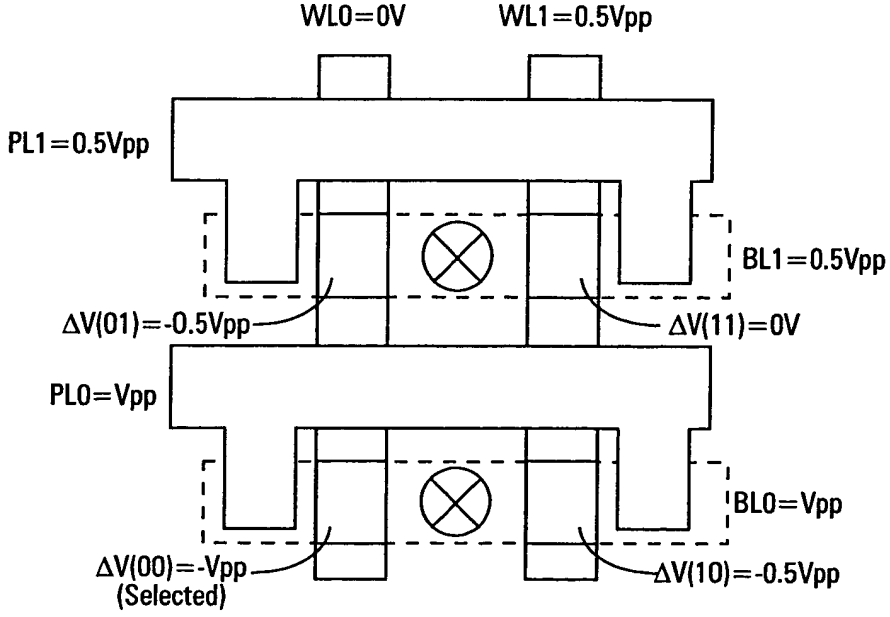
WL0=0V
WL1=0.5Vpp
PL1=0.5Vpp
BL1=0.5Vpp
ΔV(01)=-0.5Vpp
ΔV(11)=0V
PL0=Vpp
BL0=Vpp
ΔV(00)=-Vpp
(Selected)
ΔV(10)=-0.5Vpp

Fig. 7B

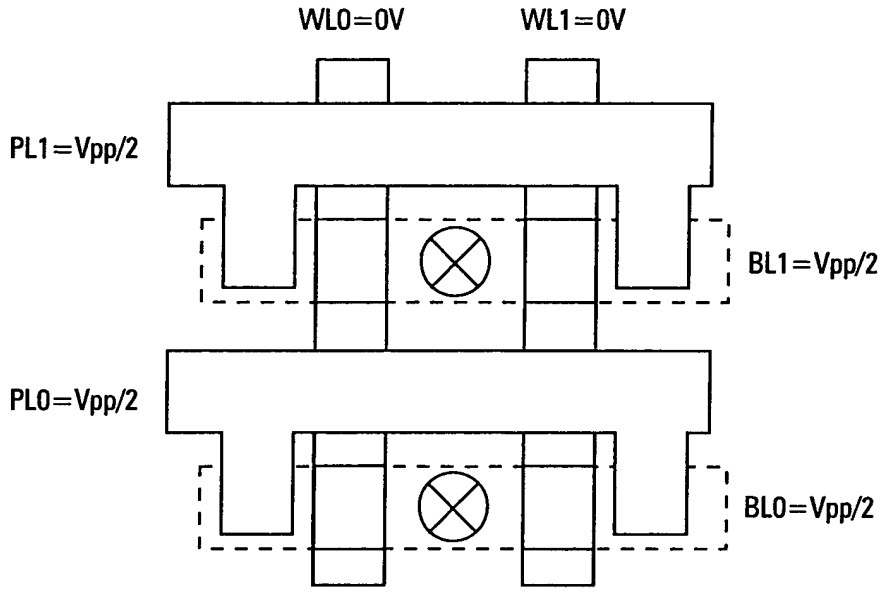
WL0=0V
WL1=0V
PL1=Vpp/2
BL1=Vpp/2
PL0=Vpp/2
BL0=Vpp/2

Fig. 8A

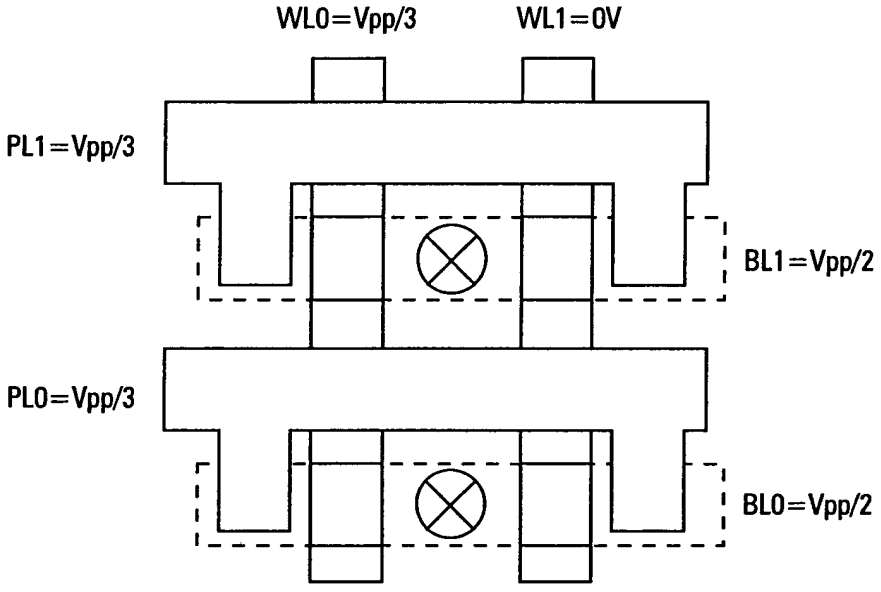
WL0=Vpp/3
WL1=0V
PL1=Vpp/3
BL1=Vpp/2
PL0=Vpp/3
BL0=Vpp/2

Fig. 8B

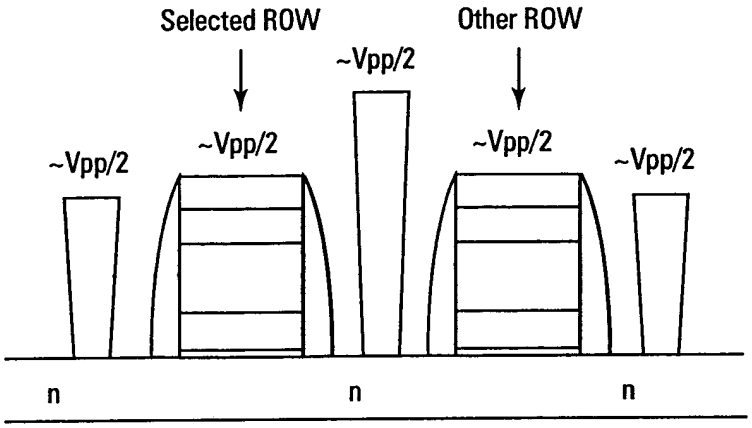

Fig. 9A

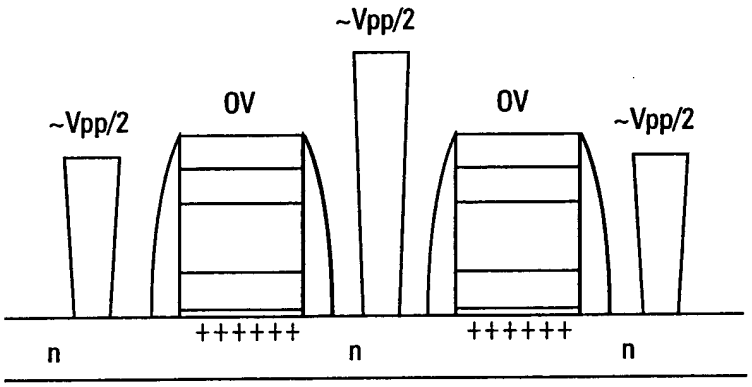

Fig. 9B

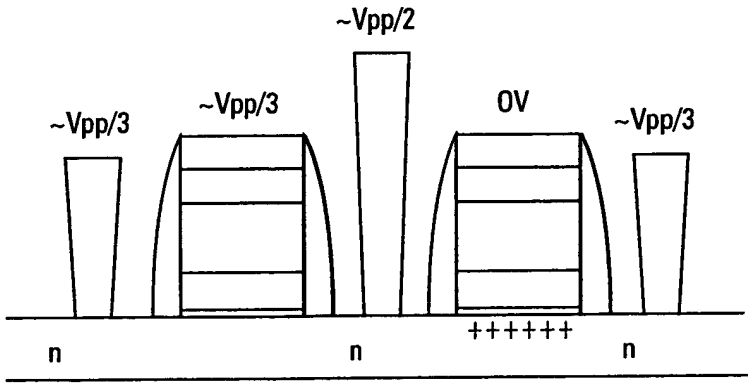

Fig. 9C

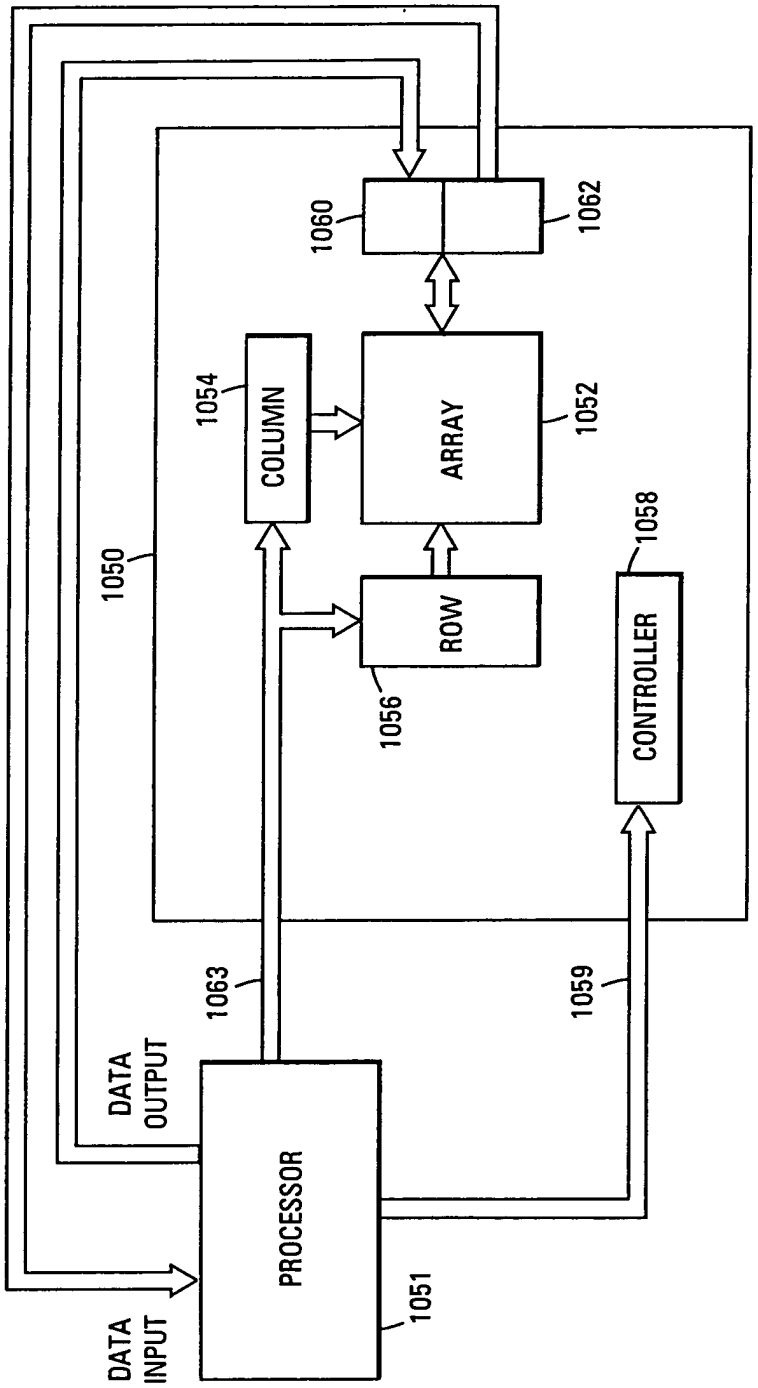
1060
1062
1054
COLUMN
ARRAY
1052
1050
ROW
1056
1058
CONTROLLER
1063
1059
DATA OUTPUT
PROCESSOR
1051
DATA INPUT

Fig. 10